Amendments to the Claims

1. (*Previously Presented*) Method for fabrication of a memory cell, for storing at least one bit, on a semiconductor substrate, comprising on said substrate a first floating gate stack (A), a second floating gate stack (B) and an intermediate access gate, said first and second floating gate stacks comprising a first gate oxide layer a floating gate, a control gate, an interpoly dielectric layer , a capping layer and side-wall spacers, said first gate oxide layer being located on said substrate, said floating gate being on top of said first gate oxide layer, said interpoly dielectric layer being on top of said floating gate, said control gate being on top of said interpoly dielectric layer, said capping layer being on top of said control gate, said memory cell further comprising source and drain contacts, said method of fabrication comprising:

defining said first and second floating gate stacks in the same processing steps to have substantially equal heights;

depositing a poly-Si layer over said first and second floating gate stacks, said poly-Si layer being deposited in between said first and second floating gate stacks in a thickness equal to or larger than the height of said first and second floating gate stacks;

planarizing said poly-Si layer by chemical mechanical polishing to obtain a planarized poly-Si layer, using said capping layer of said first and second floating gate stacks as a polish stop layer;

defining said intermediate access gate in said planarized poly-Si layer by a masking step with an access gate mask over said planarized poly-Si layer between said first and second floating gate stacks and an etching step for poly-Si.

2. (*Previously Presented*) Method for fabrication of a memory cell, according to claim 1, characterized by:

forming on top of said intermediate access gate a first self-aligned silicide area and on top of said source and drain contacts a second self-aligned silicide area;

forming on said second self-aligned silicide area a local interconnect;

depositing on top of said local interconnect, said first self-aligned silicide area, and said capping layer a pre-metal dielectric layer;

forming a contact opening in said pre-metal dielectric layer to said local interconnect;

filling said contact opening with a metal contact to said local interconnect; and

defining on top of said pre-metal dielectric layer at least one metal line as a bit-line.

3. (*Previously Presented*) Method for fabrication of a memory cell, according to claim 1, characterized by:

forming on top of said intermediate access gate a first self-aligned silicide area and on top of said source and drain contacts a second self-aligned silicide area;

depositing on top of said second self-aligned silicide area, said first self-aligned silicide area and said capping layer a pre-metal dielectric layer;

forming a contact opening in said pre-metal dielectric layer to said second self-aligned silicide area;

filling said contact opening with a metal contact to said second self-aligned silicide area; and

defining on top of said pre-metal dielectric layer at least one metal line as a bit-line, said bit-line being slanted.

4. (*Previously Presented*) Method for fabrication of a memory cell, according to claim 1, characterized by:

forming on top of said intermediate access gate a first self-aligned silicide area and on top of said source and drain contacts a second self-aligned silicide area;

depositing on top of said second self-aligned silicide area, said first self-aligned silicide area and said capping layer a pre-metal dielectric layer;

forming a contact opening in said pre-metal dielectric layer to said second self-aligned silicide area;

filling said contact opening with a contact to said second self-aligned silicide area; and

defining on top of said pre-metal dielectric layer in a first metal level said bit-line for connecting to said contact opening (CO), said bit-line being slanted.

5. (*Previously Presented*) Method for fabrication of a memory cell, according to claim 4, characterized by:

forming on top of said intermediate access gate a first self-aligned silicide area and on top of said source and drain contacts a second self-aligned silicide area;

depositing on top of said second self-aligned silicide area, said first self-aligned silicide area, and said capping layer a pre-metal dielectric layer;

forming a contact opening in said pre-metal dielectric layer to said second self-aligned silicide area;

filling said contact opening with a contact to said second self-aligned silicide area; and

defining on top of said pre-metal dielectric layer in said first metal level a landing pad on top of said contact for connecting to said contact opening by means of:

depositing an intermetal dielectric layer,

forming a further contact opening as a via opening in said intermetal dielectric layer,

filling said via opening with a contact acting as a via, and

defining in a second metal level a further slanted bit-line on top of said intermetal dielectric layer for connection to said contact acting as a via, said contact acting as a via being connected to said landing pad.

6. (*Previously Presented*) Method for fabrication of a memory cell, according to claim 1, characterized by:

said floating gate FG consisting of a trapping medium,

said trapping medium comprising an ONO layer stack, an oxygen-rich silicon layer, or a silicon dioxide layer comprising silicon nanocrystals dispersed therein.

7. (*Cancelled*)

8. (*Cancelled*)

9. (*Currently Amended*) An array of memory cells, wherein the array of memory cells includes a memory cell, for storing at least one bit, on a semiconductor substrate, comprising on said substrate a first floating gate stack, a second floating gate stack and an intermediate access gate, said first and second floating gate stacks comprising a first gate oxide layer, a floating gate, a control gate, an interpoly dielectric layer, a capping layer and sidewall spacers, said first gate oxide layerbeing located on said substrate, said floating gate being on top of said first gate oxide layer, said interpoly dielectric layer being on top of said floating gate, said control gate being on top of said interpoly dielectric layer, said capping layer being on top of said control gate, said memory cell further comprising source and drain contacts, characterized in that

said first and second floating gate stacks have substantially equal heights;

said intermediate access gate comprises a planarized poly-Si layer in between said first and second floating gate stacks,

wherein the memory cell further includes,

a first self-aligned silicide area formed on top of said intermediate access gate and a second self-aligned silicide area formed on top of said source and drain contacts;

a local interconnect formed on said second self-aligned silicide area;

a pre-metal dielectric layer deposited on top of said local interconnect, deposited on top of said first self-aligned silicide area, and deposited on top of said capping layer;

a contact opening formed in said pre-metal dielectric layer to said local interconnect;

said contact opening filed with a metal contact to said local interconnect; and

at least one metal line defined as a bit-line on top of said pre-metal dielectric layer; and

~~Array of memory cells according to claim 8, characterized in that~~

~~said~~ the memory array includes at least two adjacent memory cells ~~are~~ arranged in a virtual ground arrangement; and

in said virtual ground arrangement a bit-line is a metal line; said bit-line being connected to said second self-aligned silicide area by a contact in said contact opening.

10. *(Previously Presented)* Array of memory cells according to claim 9, characterized in that in said array of memory cells at least two memory cells connect to said contact opening for said bit-line.

Claims 11-12 *(Cancelled)*

13. *(Previously Presented)* Array of compact memory cells, according to claim 10, characterized in that said bit-line is slanted and connected to memory cells, which are not horizontally neighboring cells having the same control gate.

14. *(Previously Presented)* Array of compact memory cells according to claim 10, characterized in that

in a first metal deposition process level (metal-1) said bit-line as a metal-1 bit-line comprises a plurality of first line parts running in a direction parallel to said active lines and a plurality of second line parts, each of said first line parts being formed on top of one of said contacts, said second line parts being formed in between said contacts, and

in a second metal deposition process level (metal-2) said bit-line as a metal-2 bit-line comprises a plurality of first line parts running in a direction parallel to said active lines and a plurality of second line parts, each of said first line parts being formed on top of one of said contacts acting as a via, said second line parts being formed in between said contacts acting as a via;

said bit-line running step-wise for connecting to memory cells, which are not horizontally neighboring cells having the same control gate, with each of said second line parts running in a direction perpendicular to said active lines or running in a slant direction relative to said active lines.

15. *(Cancelled)*